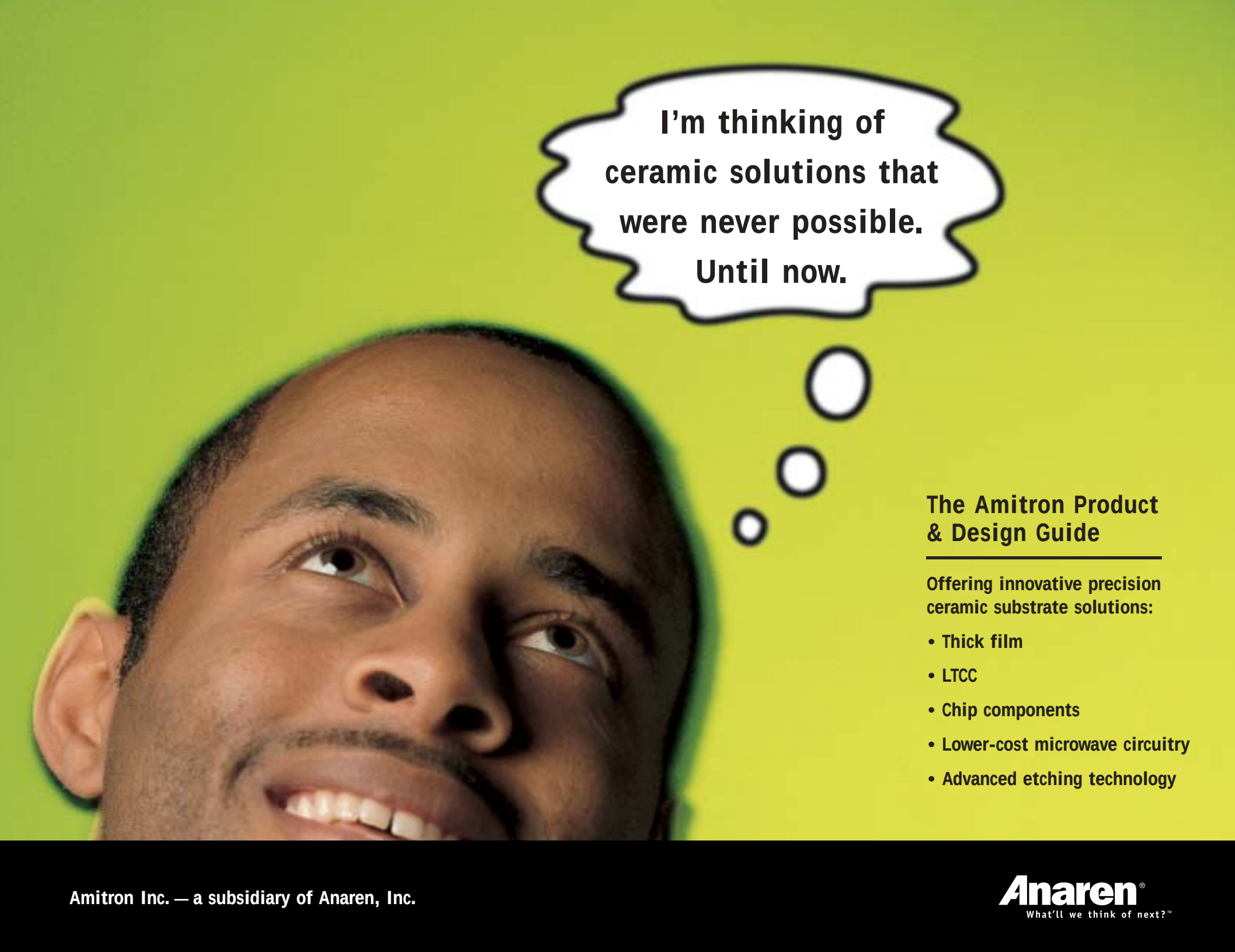

The Amitron Product & Design Guide

Offering innovative precision ceramic substrate solutions:

- Thick film
- LTCC
- Chip components
- Lower-cost microwave circuitry
- Advanced etching technology

Amitron Inc. — a subsidiary of Anaren, Inc.

Anaren®
What'll we think of next?™

> Contents

> About this Product & Design Guide

This Product & Design Guide reflects the current capabilities of Amitron's facility and experience. We've provided it to assist you in the initial evaluation of your design's compatibility with the various thick film technologies we offer — as well as to introduce you to methods, processes, and techniques that can minimize costs and cycle times.

This guide does not represent the full range of possibilities of our fast-expanding and continually improving technologies, nor does it replace the interaction between customers and Amitron's engineers; this dialogue is welcome and needed to provide the most robust and cost-effective design.

> Contact

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> About us

Amitron Founded in 1985, and added to the Anaren team in 2001, Amitron is a leading manufacturer of quality thick film circuits. From multilayer substrates and LTCC, to lower-cost microwave circuitry featuring etched conductors, chip resistors and attenuators, and more — Amitron is your innovator in thick film processing. Our specialties include:

> **Exclusive, ceramic-based thick film solutions,** whatever your product requirements. A wide variety of the latest technologies and materials, along with the engineering experience to utilize them adeptly and ingeniously, enable us to provide solutions other suppliers simply can't.

Of particular interest is our recently added full-service LTCC capability, featuring DuPont, Ferro, and Heraeus material systems ... names you can count on.

In the area of substrates, Amitron solutions include features such as filled substrate vias, edge wraps, integrated resistors, capacitors, and inductors. And throughout, we employ the latest thick film pastes — and a variety of substrate materials such as alumina, aluminum nitride, beryllia, and ferrite for maximum design flexibility.

> **Vertical integration.** Need design assistance, ceramic machining, thick film screening, or LTCC manufacturing? How about etching, plating, laser trimming, and comprehensive product testing? Amitron offers it all under one roof — for reduced costs, speedier turn times, and the advantages of shared information across disciplines.

> **Products for a diverse customer base.** At Amitron, we work with customers in medical, wireless, optical, automotive, aerospace, aviation, and other industries.

The varied and exacting demands of these sectors have made us proficient in developing all kinds of low-cost, quick-turn prototypes. They have also enabled us to compress our design-to-production cycle times; match our capacity to your low- or high-volume manufacturing needs; and develop a range of quality "stock" products, including microwave chip attenuators and the industry's smallest wire-bondable chip resistors (20 x 20 mils), to very high-performance specs.

> **The added confidence of Anaren engineering.** If your project calls for specialized microwave circuit design know-how in addition to Amitron's manufacturing capabilities, count on our parent company: Anaren. Results can include reduced costs and time-to-market.

So if you're thinking of solutions never before possible, think Amitron! Start with this Product & Design Guide for data, specifications, and drawings — then call us at 978-686-1882 when you need the expertise, experience, and capabilities to make those solutions real.

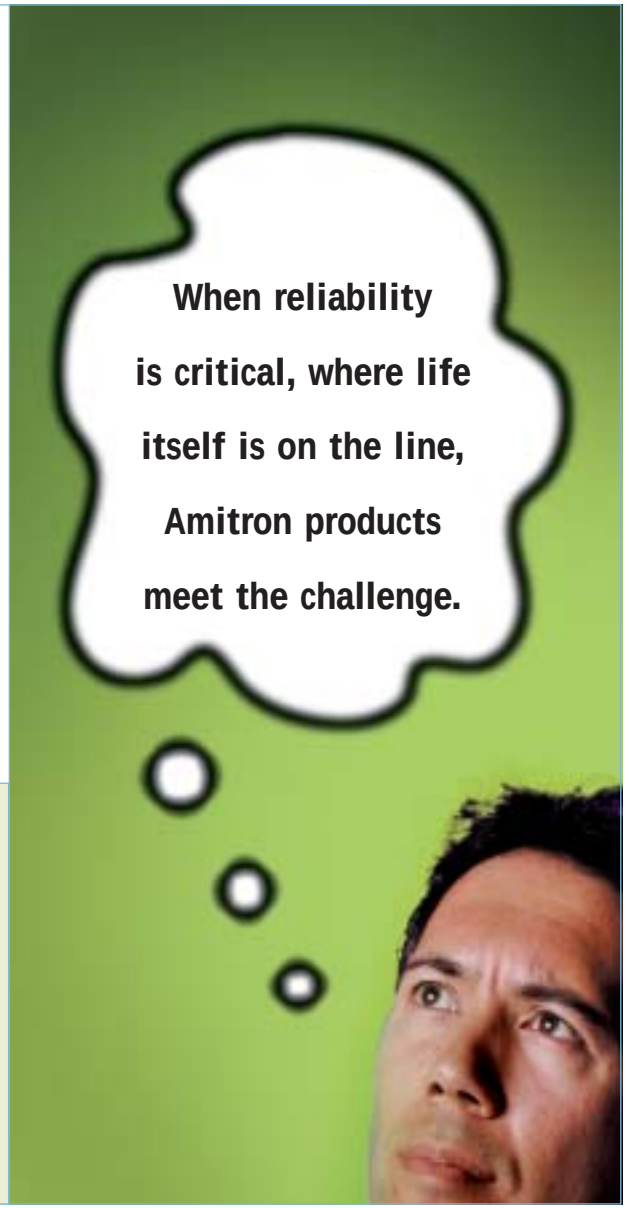
Product quality assurance:

> **ISO 9002 registered**

> **Quality requirements MIL-Q-9858**

> **QPL listed chip resistors MIL-PRF-55342**

> **Test capabilities MIL-PRF-38534**



Highlights:

- > Sequentially applied layers of alternating conductor and dielectric to build up the multilayer structure
- > Typically used for one to eight conductor layers per side (single or double sided)
- > A selection of metals for wirebonding, soldering, brazing
- > Integrated resistors, capacitors, inductors
- > Alumina, ferrite, aluminum nitride, beryllia substrates, and more
- > Wide range of resistor materials and values on a single substrate
- > Wraps and metallized substrate vias
- > Advanced substrate machining, including various shapes and cutouts
- > Combine with etched thick film and LTCC if needed

Conductors

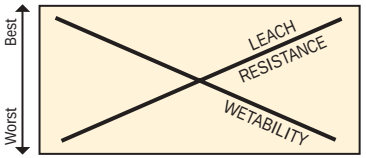
> Fritless golds are used for high-reliability conductors and for gold wire bonding. Fritted gold metallizations have higher adhesion to the substrate and, for that reason, are often substituted for fritless gold. Pt/Au and Pt/Pd/Au alloys have very high solder leach resistance and are used for critical solderable applications.

Pure silvers have the lowest resistivity, and when alloyed with palladium and/or platinum, become increasingly leach resistant. Careful silver alloy selection will produce a high-reliability part in cost-sensitive applications. Special acid-resistant alloys of silver are used as the base metal for nickel barrier plating when the ultimate in solder leach resistance is required.

Conductor Properties

	Gold	Platinum/ Gold	Silver	Palladium/ Silver	Platinum/ Silver
Relative Cost*	20-25	25-30	1	2-5	1-5
Sheet Resistivity (mΩ/sq)	3-7	60-100	1-2	10-50	4-5
Solderability (Sn/Pb)** **Leach Resistance****	4 1	2 5	5 1	2-4 3-4	3-4 2-3
Typical Fired Thickness (mils)	0.3-0.5	0.4-0.6	0.4-0.7	0.4-1.0	0.4-0.6
Typical Line Resolution (width/space in mils)	5-7 1***	7-10	7-10	7-10	7-10

* Relative Cost: 1 = Lowest ** Relative Values: 5 = Best *** Etched Thick Film



INCREASING ALLOY (Palladium or Platinum)

Dielectric

> Thick film dielectrics are designed to be used as insulators between conductor layers in crossover and multilayer applications. Overglazes are used as protective coatings over printed resistors and capacitors. They also serve as solder stops in surface mount assemblies and provide protection from harsh chemicals in the plating process.

Dielectric Properties

	Dielectric Constant	Dissipation Factor	Breakdown Voltage (V/mil)	Fired Thickness (mils)	Insulation Resistance (ohms)
Standard	6-12	< 0.5%	500	1.5-2.0	$>10^{11}$ @ 100 V
Low - K	3.9	<0.01% 0.04% @ 20 GHz	500	1.0-2.0	$>10^{11}$ @ 100 V

Resistors

> Standard resistor materials are made from glasses and oxides of ruthenium metal. Sheet resistivities are available from milliohms to gigaohms and can be combined on a single substrate. Standard trim tolerances are 10% through 1%, and in some cases to 0.5%. Large numbers of minimum size resistors on a substrate may be limited to 5% to 10%.

Typical Resistor Characteristics

	SHEET RESISTIVITIES (OHMS /SQUARE)							
	1	**10**	**100**	**1K**	**10K**	**100K**	**1M**	**10M**
TCR (PPM/C) Maximum	300	300	300	300	300	300	300	300
Typical	150	100	100	100	100	100	100	100
Available	-	50	50	50	50	50	50	-
Standard Working Voltage (V/Mil)	0.02	0.07	0.20	0.70	2.0	2.0	4.0	10.0
Maximum Rated Power Dissipation[1] (W/in^2)	325	500	500	500	500	250	100	10

[1] Laser trim will reduce resistor area by up to 50%

Capacitors

> Capacitors are processed using standard screen printing techniques and fired directly onto the surface of the substrate. They may also be buried within or on top of multilayer structures. Electrodes must be of the same material. Typical dielectric thickness is 40 microns. Capacitor tolerances to 2% in some cases.

Typical Printed Capacitor Properties

Dielectric Constant (K)	20-50	100-300	500-750	750-1500
Dissipation Factor (1 kHz)	< 0.3%	< 1.0%	< 1.2%	< 3%
Dissipation Factor (1 MHz)	< 0.5%	< 1.6%	< 2.0%	-
Dielectric Strength (Volts/mil)	> 500	> 500	> 500	> 500
Insulation Resistance (Ω @ 100 V, 1 kHz)	$> 10^{11}$	$> 10^{11}$	$> 10^{11}$	$> 10^{9}$
TCC (ΔC, 25°C-125°C)	< 3%	< 6%	< 15%	(Z5U)

Typical properties based on 0.100" x 0.100" capacitor

Substrates

> Standard substrate materials include alumina (Al_2O_3) in sizes to 6" x 4", aluminum nitride (AIN) in sizes to 4" x 4", and beryillia (BeO) in sizes to 2.3" x 2.9". Laser scribing 0.025"-thick rectangular alumina provides the most effective approach to meeting mechanical requirements. When necessary, substrates can be machined to produce virtually any shape. Other available substrate materials include aluminum nitride, ferrite, silicon carbide, quartz, and sapphire. Standard thicknesses 10 to 60 mils, ±10%. Standard camber 3 mils/inch max. Increased control of thickness, camber, and surface finish is available by lapping or polishing.

Substrate Material Characteristics

	Unit	**96% Alumina**	**99.5%/99.6% Alumina**	**Beryllia (BeO)**	**Aluminum Nitride (AIN)**
Dielectric Constant	1MHz	9.5	9.9	6.5	8.6
Dissipation Factor	1MHz	0.0004	0.0001	0.0004	0.001
Thermal Conductivity (100°C)	W/m-K	20	27	270	170
Coeff. Thermal Expansion	ppm/°C	6.3-8.0	7.0-8.3	9.0	4.6

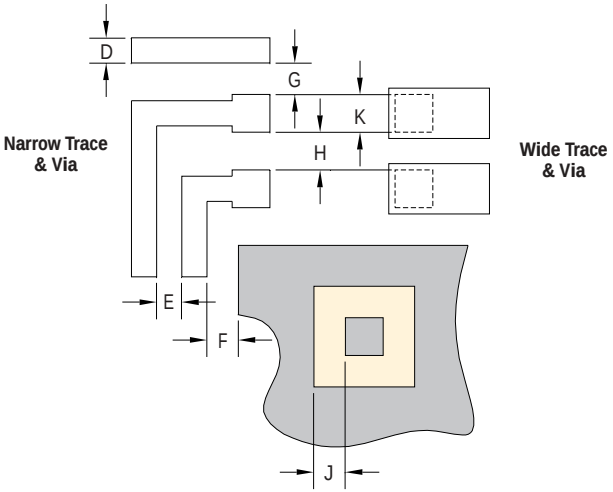
Standard Thickness	inch	0.010 0.015 0.020 0.025 0.040 0.060 (others available)

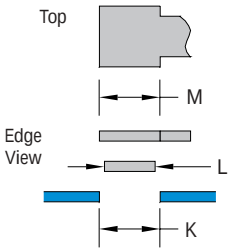
Thick film multilayer design rules follow on the next several pages.

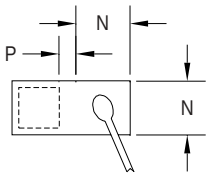
> Minimum and standard feature sizes are shown. All features can be of greater size unless otherwise indicated.

> Feature sizes greater than the minimum improve producibility.

Conductors & vias





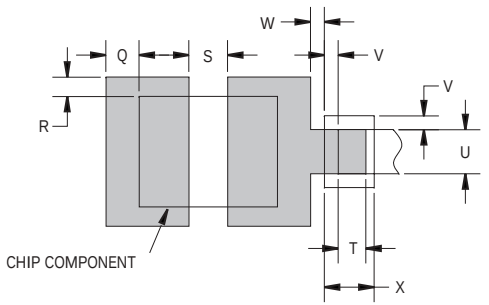


	Rule	Fine-Line Gold Minimum (mils)	Fine-Line Gold Standard (mils)	Other Golds & Silvers Minimum (mils)	Other Golds & Silvers Standard (mils)
D	Conductor Width	5	7	7	10
E	Conductor Spacing	5	7	7	10
F	Conductor Spacing Different Materials	7	10	10	12
G	Conductor to Via	8	10	10	12
H	Via to Via, Isolated	10	15	12	15
J	Conductor Isolation in Power/Ground Plane	7	10	10	12

	Rule	Minimum (mils)	Standard (mils)
K	Via Size (dielectric opening)	10	15
L	Via Fill[1]	9	14
M	Conductor Over Via[2]	10 x 10	15 x 15
N	Wirebond Pad Size (for 1 mil Gold Wire)	10 x 10	10 x 14
P	Via to Wirebond Pad[3]	5	

[1] Via fill 1/2 mil smaller than via opening, all around
[2] Minimum size same as via size
[3] This spacing improves planarity of wirebond site

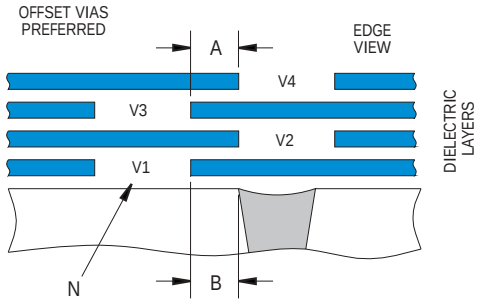
Solder pads & gold/silver interface

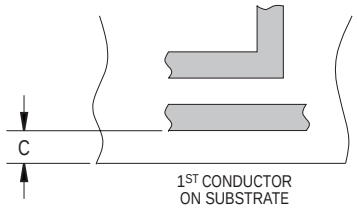


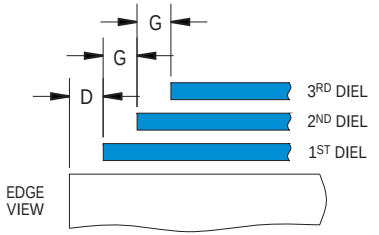
	Rule	Minimum (mils)	Standard (mils)
Rules Q-S: Solder Pads[4]			
Q	Chip Pad Extension, Length	10	12
R	Chip Pad Extension, Width	5	7
S	Solder Pad Spacing	15	-
Rules T-X: Au-Ag Interface where required[5]			
T	Overlap Length, Dissimilar Materials	8	12
U	Overlap Width, Dissimilar Materials	10	12
V	Solder-Stop Overlap at Gold-Silver Interface	5	7
W	Glaze (solder mask) Stepback	2	5
X	Glaze Width	8	15

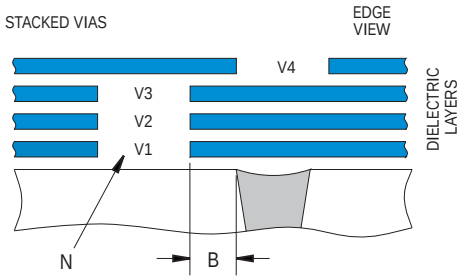
[4] Suggested dimensions
[5] Non-alloyed gold must be protected from the leaching effects of solder

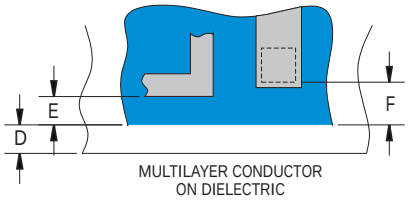
Vias, dielectrics & crossovers

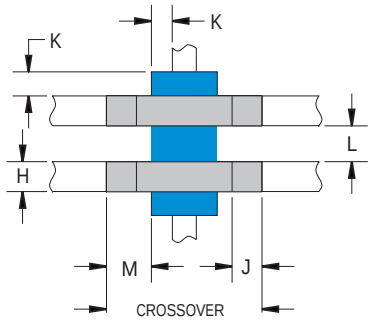










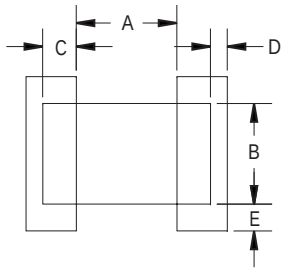


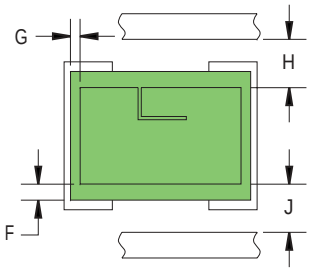
	Rule	Minimum (mils)	Standard (mils)
N	Via Stacking	3 MAX	Offset
A	Offset Via Spacing	0	5
B	Via to Filled Substrate Hole	3	5
C	Conductor to Snapped Substrate Edge	8	10
	Conductor to Diced Substrate Edge	2	5

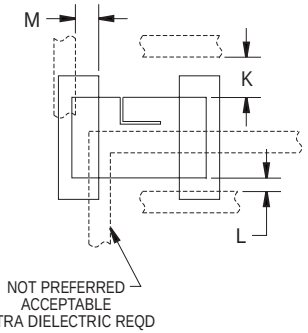
	Rule	Minimum (mils)	Standard (mils)
D	Dielectric to Snapped Substrate Edge	8	10
	Dielectric to Diced Substrate Edge	2	5
E	Multilayer Conductor to Dielectric Edge	7	10
F	Via to Dielectric Edge	10	15
G	Dielectric Stepback	2	5

	Rule	Minimum (mils)	Standard (mils)
Rules H-M also apply to conductors running off the edge of a dielectric			
H	Crossover Width	10	12
J	Crossover Overlap	8	12
K	Dielectric Overlap	7	10
L	Crossover Spacing	10	12
M	Crossover Length Beyond Dielectric	8	15

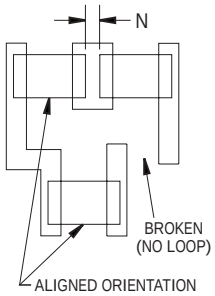
Printed resistors



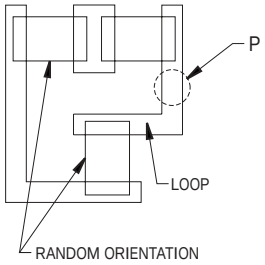




	Rule	Minimum (mils)	Standard (mils)
A	Resistor Length	15	30
B	Resistor Width	15	30
C	Resistor / Termination Overlap	7	10
D	Termination Extension (Length Direction)	3	5
E	Termination Extension (Width Direction)	5	8
F	Overglaze Coverage, Width[1]	5	8
G	Overglaze Coverage, Length	0	3
H	Conductor to Trimmed Resistor Edge	15	20
J	Conductor to Untrimmed Resistor Edge	10	15
Rules K-N apply to 1ST layer below resistor			
K	Buried Conductor to Trimmed Resistor Edge	15	20
L	Buried Conductor to Untrimmed Resistor Edge	0	5
M	Buried Conductor to Resistor Along Termination	10	15
N	Resistor to Resistor on Common Termination[2]	7	10
P	Resistor Probe Pad[3]	10 x 10	15 x 15
-	Resistor Orientation[4]	Random	Aligned
-	Resistor Loops[5]	Loop	No Loops



PREFERRED



ACCEPTABLE

1 Overglaze used where environmental stability is required

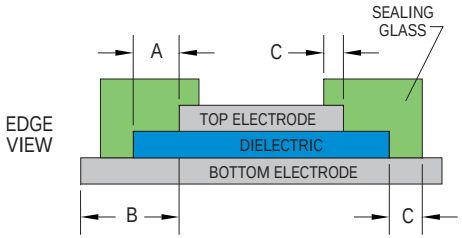
2 Zero spacing allowed if both resistors use same paste

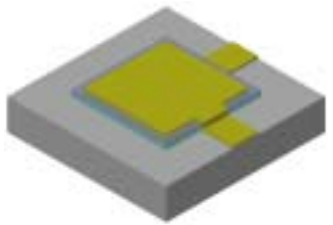
3 Probe pad not covered by glaze or dielectric; located anywhere on trace; not in area reserved for termination extension

4 Orienting resistors in the same direction is especially helpful for small-geometry resistors

5 Identify resistor loops in drawing notes

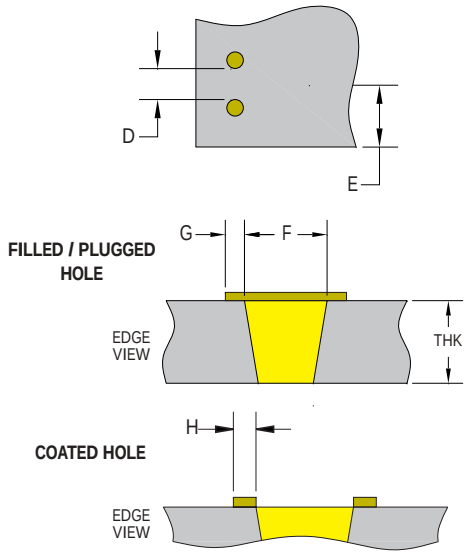
Printed capacitors

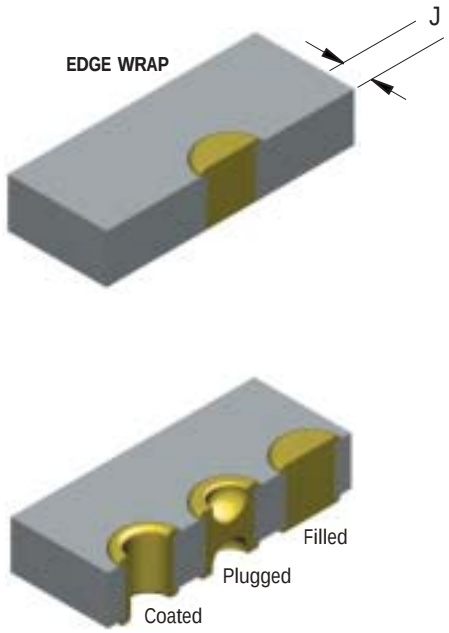




	Rule	Minimum (mils)	Standard (mils)
A	Dielectric Overlap Smaller Electrode	7	10
B	Larger to Smaller Electrode Overlap	0	5
C	Sealing Glass/ Dielectric Overlap	5	7

Holes and edge wraps





	Rule	Minimum (mils)	Standard (mils)
D	Hole Spacing (Edge to Edge)	>= 0.5 x Sub Thk	>= 1.0 x Sub Thk
E	Hole to Snapped Substrate Edge	>= 0.75 x Sub Thk & >= Hole Dia	>= 1.0 x Sub Thk & >= Hole Dia
	Hole to Diced Substrate Edge	>= 0.5 x Sub Thk	>= 1.0 x Sub Thk
-	Substrate L & W Tolerance, Diced Edge	± 2	± 4
-	Substrate L & W Tolerance, Snapped Edge	± 5	± 10

	Rule	Minimum (mils)	Standard (mils)
F	Plugged/Filled Hole Diam, 0.010-0.025 thk Substrate	-	7
	Plugged/Filled Hole Diam, 0.030-0.040 thk Substrate	-	8
	Plugged/Filled Hole Diam, 0.050-0.060 thk Substrate	-	10
G	Conductor Overlap Hole	5	7
H	Coated Hole Annular Ring Width	7	10
J	Wrap onto Top or Bottom Surface	15	20

Customer drawings and CAD files

> For any design work (thick film multilayer, etched thick film, or LTCC), customer CAD files are preferred in one of the following formats:
- Autocad .DWG
- .DXF
- CADKEY .PRT
- Additionally, files using Gerber RS-274X format can be processed

> High-density designs are best tested using a customer-furnished netlist having:
- ASCII format
- Nets by name or number
- Node X, Y locations
- Measure (mils, inch, mm)
- (0,0) location

> Paper drawings, or their CAD equivalents, should indicate special requirements. Where resistor loops are present, it is helpful that they are highlighted. Using revision control on documents helps ensure design changes are captured.

> In all cases, an active dialogue between you and your Amitron team ensures that design requirements and applications intents are met!

Microwave structures can be integrated onto your substrate

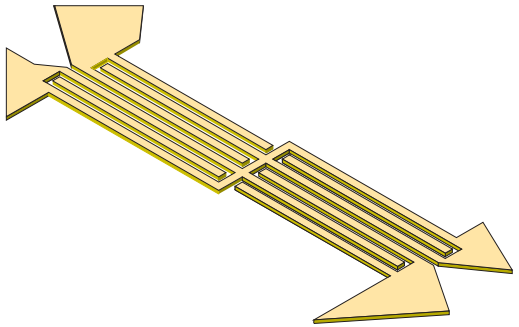
> Filters, inductors, microstrips, Lange couplers with crossovers

> Etched thick film gold or silver conductors

> Excellent line edge definition, +/- 0.2 mil or better

> An innovative combination of thin film photoimaging technology and advanced thick film materials produces high-performance, cost-effective microwave circuits.

> Thin film performance at thick film costs — up to 40% savings over thin film

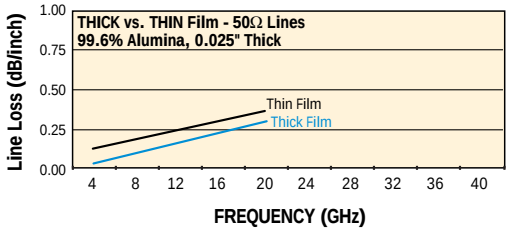


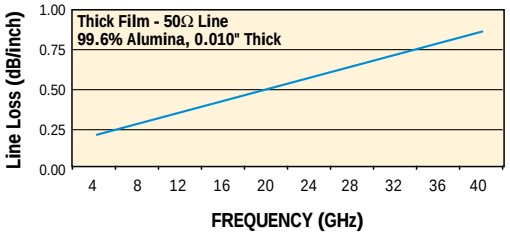
Combine etched features with multilayer features

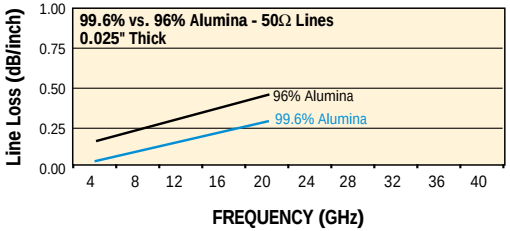
> Capacitors, resistors, hole fill, wraps, solder- and braze-metallizations

> Alumina (96%, 99.5%, 99.6%), ferrite, aluminum nitride, quartz substrates

> Standard and low-K dielectrics

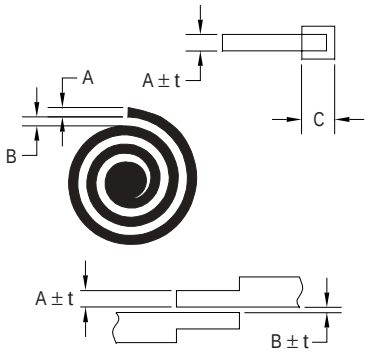






And use etched thick film to achieve high-density interconnect

ETCHED CONDUCTORS



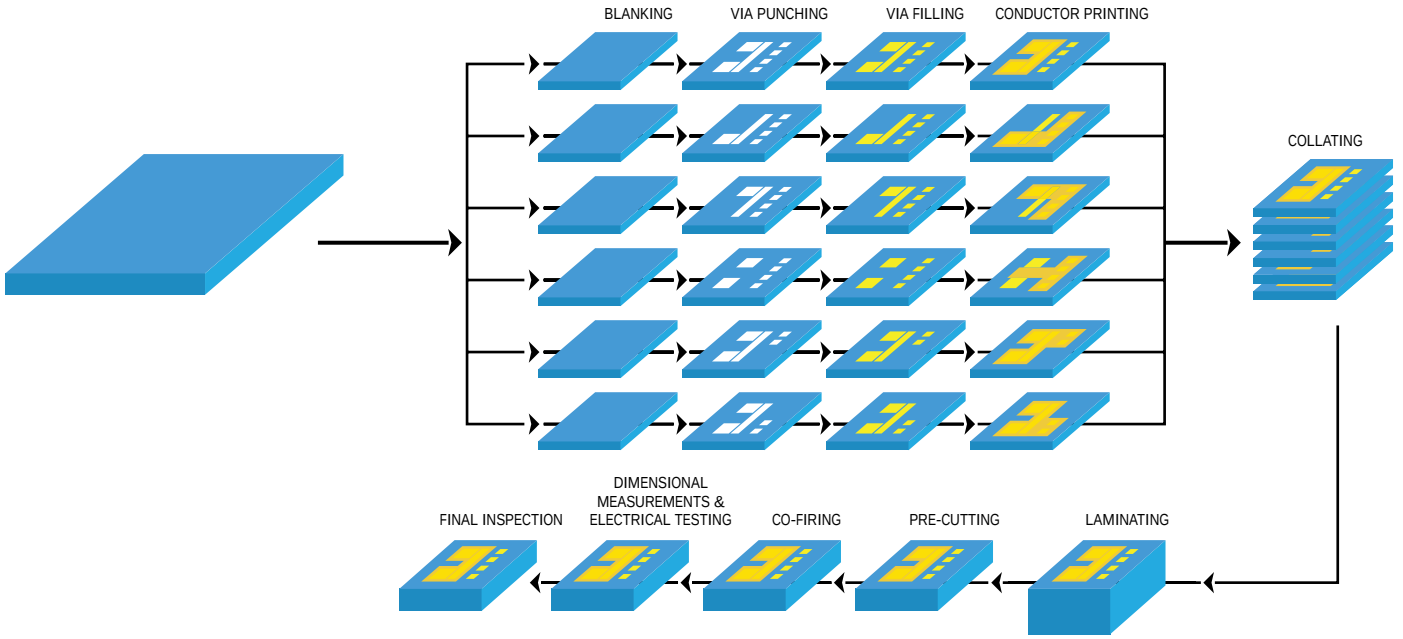
	Rule	Minimum (mils)	Standard (mils)
A	Conductor Width	1	2
B	Conductor Spacing Same Print Mask	1	2
C	Via Size (Dielectric Opening)	2 x 2	3 x 3
t	Line Width Tolerance	0.15	0.20

Overview

> Amitron offers Low Temperature Co-fired Ceramic (LTCC) technology as an attractive solution for high-density multilayer networks and high-frequency applications. Amitron supplies the customer with a totally integrated solution to real-world problems by employing any and all of the following:

> Integrated components
> Etched thick film technology
> Photolithographic technology
> Passive element tuning by YAG laser
> 100% continuity testing
> Brazing capabilities

> Below is a pictorial representation of the LTCC manufacturing process. As shown, LTCC is a parallel process allowing for complex, high-density designs with high reliability and excellent mechanical and electrical properties.



Terms

> Tape

A combination of dielectric and ceramic material is cast onto a Mylar® (or similar) backing material at a precise, controlled thickness. This material acts as an electrical isolation between concurrent electrical pathways and exhibits controlled, predictable shrinkage in the XYZ axes when laminated and fired at the proper time-temperature profile. Tape and pastes in an unfired condition are defined to be in the “green state.”

> Co-fired materials

Each materials vendor supplies via fill and conductor materials (with other material types available) matched to shrink in conjunction with green tape dielectric. Such materials are fired a single time along with the LTCC tape.

> Post-fired materials

After the LTCC firing operation, some materials are available from each vendor to print and fire using thick film technology on the surfaces of the LTCC material. Such materials are subject to the same processing restrictions as when they are used in thick film multilayer technology.

> Blanking

A steel die may be used to cut the green state outline and (possibly) an orientation mark to indicate how the material was removed from the roll.

> Via punching

With a mechanical multi-punch tool, interconnection points between layers as well as collating holes are punched in the green state tape.

> Via filling

A high-solids-content material is used to provide electrical and thermal interconnection between the isolation layers of the green tape. Several techniques and processes may be used depending on the material, as well as the specific design.

> Conductor printing

An automated optical alignment screen printer is used to apply the appropriate conductive materials to the surface of the green tape.

> Photolithography (optional)

If required by the design, a photosensitive process may be used to process extremely fine lines in the conductive pattern. Currently, photosensitive green tape materials, used for high-speed via formation and complex shape and cavity generation, are under development by several vendors.

> Cavity formation (optional)

For those designs requiring a 3D final structure, the cavities in each layer are applied using either a mechanical punch or photolithographic techniques.

> Collating

Through either an automated optical alignment system or a mechanical pinning system, the layers are stacked in the correct order and held in place during the lamination process.

> Lamination

Through an isostatic lamination system, the collated green tape part is typically subjected to 3,000 psi under controlled temperature and time to complete the green state process.

> Firing

Through either a belt furnace (products with thickness less than 120 mils after firing) or a programmable box furnace, the green state parts are subjected to a controlled time-temperature profile to complete the majority of the product sintering process. The result is a final product with predicted XYZ shrinkage and of appropriate density and characteristics to meet final electrical requirements.

> Electrical test

A typical test inspection of a completed part includes an electrical open-and-short test known as a Net test. This DC electrical test is a standard procedure — RF and high-frequency test requirements must be reviewed between Amitron and the customer.

Materials

> Options for various materials can be found in Tables 1 and 2. These options cover the most popular, currently available materials for tape, gold metal systems, silver metal systems, and mixed metal systems.

> Specific material choices are highly dependent upon the circuit electrical, physical, and environmental requirements, as well as the specific processing operations to be performed on the final board. Cost is also a factor that may impact the choice of specific materials used in the final design.

> Additionally, current and new vendors are continually developing materials for various applications. Final materials selection and recommendations should be the result of collaboration between the customer and the appropriate engineers.

> Key features for gold metal systems, silver metal systems, and mixed metal systems are listed in Table 3 on page 14.

Table 1: Dielectric/Tape Base Material Features

Manufacturer	DuPont		Ferro	Coors
Feature	**951**	**943**	**A6-M**	**96% Al_2O_3 (Ref.)**
Fired Thickness (per layer)	951C2 45 µm 951PT 95 µm 951P2 135 µm 951PX 210 µm	A5 110 µm	-5 95 µm -10 190 µm	N/A
Average K @ 1MHz	7.8	7.4	5.9	9.2
Loss Tangent @ 40 GHz **Dissipation Factor** @ 1 MHz	0.0240 0.15%	0.0020 0.09%	0.0020 0.20%	0.0015 0.30%
Insulation Resistance, Single Tape Thickness	> 10^{12} ohms	> 10^{12} ohms	> 10^{12} ohms	> 10^{14} ohms
Breakdown Voltage Per 25 µm Thickness **Fired Density**	> 1000 VDC 3.1 g/cm^3	> 1100 VDC 3.2 g/cm^3	> 800 VDC 2.5 g/cm^3	> 2500 VDC 3.6 g/cm^3
Typical R_a Surface Finish	< 10 µ-in.	< 25 µ-in.	< 10 µ-in.	< 25 µ-in.
Fracture Strength	320 MPa	230 MPa	130 MPa	400 MPa
TCE	5.8 ppm/°C	6.0 ppm/°C	7.0 ppm/°C	7.1 ppm/°C
Thermal Conductivity (Without Thermal Vias)	3.0 W/m °K	4.4 W/m °K	2.0 W/m °K	21.0 W/m °K
Potential Camber[a]	< 3 µm/cm	< 3 µm/cm	< 3 µm/cm	< 3 µm/cm

Notes: a) 8-layer laminate structure, no metalization.

Table 2: Material Options

Manufacturer	DuPont		Ferro
Process	**951**[a]	**943**	**A6-M**
Inner Layer Au	5734	HF502	30-025
Via Fill Au	5738	HF500	30-078
Wirebond Co-Fire Au	5742 (Al wire) 5734 (Au wire)	HF502 (Au wire)	30-065 (Al wire) 30-025 (Au wire)
Wirebond Post-Fire Au	5743 (Al wire) 5715 (Au wire)	5725 (Al wire) 5715 (Au wire)	30-068 (Al wire)
Solderable Au	5739 (Pt/Au)	HF515 (Pt/Au)	36-020 (Pt/Au)
Photoimageable Au	5956	5956	4002
Brazing Material (AuSn, AuGe Braze)	5062/5063	5062/5063	4007
Inner Layer Ag	6142 (Signal) 6148 (Power, Gnd)	HF612 (Signal) HF602 (Power, Gnd)	33-398
Via Fill Ag	6141 (Ag) 6138 (Pd/Ag)	HF600 (Ag) HF640 (Pd/Ag)	33-343 (Ag) 39-005 (Pd/Ag)
Solderable Co-Fired Ag	6146 (Pd/Ag)	HF615 (Pd/Ag)	33-391
Solderable Post-Fired Ag	6135 (Pd/Ag)	6160 (Pd/Ag)	3350
Co-Fired Resistors	CF Series	NCA[b]	87 Series
Post-Fired Resistors	7200 Series	NCA[b]	NCA[b]
Co-Fired Dielectric	9615	9615	10-088
Post-Fired Overglaze	QQ550	QQ550	NCA[b]
Photoimageable Dielectric	6050	6050	NCA[b]

Notes: a) A photoimageable version of the DuPont 951LTCC tape is available for complex shapes and MEMS. b) NCA = Not currently available.

Vias

> Vias in the green tape material provide electrical and/or thermal connections between consecutive layers of the material (see Figure 1). The type of via used (stacked, staggered, thermal, spreading, or hermetic) is dependent upon the specific circuit requirements for electrical and thermal performance. The via selection can have a significant impact on the overall product yield, and therefore generally represents an intelligent compromise between meeting customer requirements and maximizing manufacturability.

> Standard green state via diameters are: 125 µm, 175 µm, 250 µm, and 500 µm. Other via diameters and/or non-round punches can be employed but require ordering additional tooling with a 3- to 5-week lead time. In all cases, 500 µm is the maximum via diameter for successful via fill operations. For maximum manufacturability, via diameter should be approximately the same as the green tape thickness.

> Standard via pitch (see Figure 2) is 3 X diameter + tape thickness. Minimum center-to-center via pitch: 1.5 X diameter + tape thickness. Unless otherwise specified by design, minimum distance from via center to part edge is 3 X via diameter.

> Standard capture pads for vias: via diameter + 125 µm. Minimum capture pads for vias: via diameter + 40 µm.

> Stacked and staggered vias are recommended for most applications to minimize top metal pad non-flatness — known as "via posting" — evident after the lamination process. For thermal vias, 250 µm vias (green state, 210 µm after firing) on a 500 µm staggered grid pattern (green state, 435 µm after firing) are recommended.

> Due to the nature of via fill materials, those applications requiring hermetic packages must have one intact tape layer, or offset staggered via, between a thermal via construct and the outside package surface.

FIGURE 1: VIA DEFINITION, CROSS-SECTION

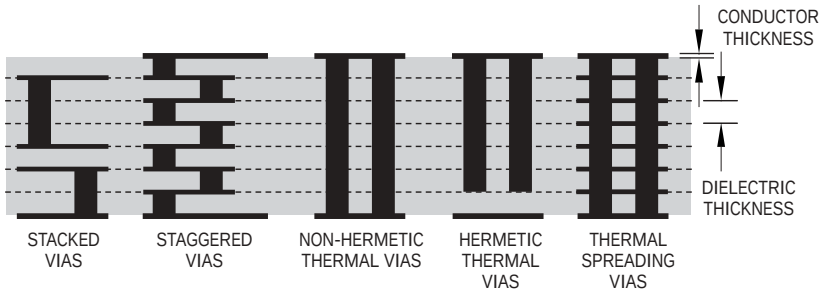
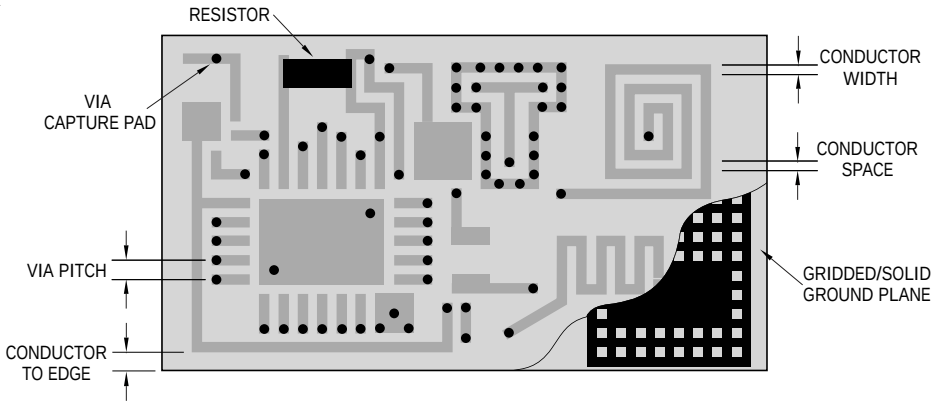


FIGURE 2: FEATURE DEFINITION, TOP VIEW



Conductors

> Minimum distance from conductor to edge (see Figure 2, page 13) is 250 µm. Minimum line and spacing capability for co-fired and post-fired conductors is defined in Table 3.

> Ground and power plane capabilities are listed in Table 3. Gridding both types of features is highly recommended to improve flatness, reduce shrinkage irregularities, improve overall structural strength and integrity, and improve manufacturabilty.

> All gold/silver interfaces, co-fired or post-fired, must employ a transition metal to prevent Kirkendall voiding. Typically the transition metal is a palladium silver material between the silver and gold conductors.

Brazing

> Conductors for successful brazing to LTCC are available for the primary tape systems. Please refer to Table 2 on page 12 for the specific material choices.

> To meet MIL Specification Visual Inspection Criteria, it is recommended that the brazing pad be 750 to 1000 µm larger than the lead or seal ring component.

> Gold-tin or gold-germanium soldering is recommended for most applications. Amitron and Anaren have soldering capability for those customers requiring a completed package.

Table 3: Design Guidelines Summary

Design Feature	Standard Guides	Premium Guides	Photolithography Guides[c]
Tape Layer Count	8-20 Layers	Up to 30 Layers[b]	Up to 30 Layers[b]
Max. Substrate Size, Fired[a]	100 mm x 100 mm	100 mm x 100 mm	100 mm x 100 mm
Conductor Lines/Spaces	150 µm min. 1-7mil	75 µm min. 3 mil	30 µm min. 1.2 mil
Via Diameter, 95 µm Tape	180 µm min. 7-8mil	125 µm min. 5 mil	125 µm min. 5 mil
Via Diameter, 215 µm Tape	320 µm min.	250 µm min.	175 µm min.
Via Capture Pad, Co-Fired	Via Φ + 125 µm	Via Φ + 40 µm	Via Φ + 30 µm
Via Capture Pad, Post-Fired	Via Φ + 200 µm	Via Φ + 125 µm	Via Φ + 110 µm
Thermal Vias, 95 µm Tape	250 µm Φ 10 mil 500 µm pitch 20 mil	125 µm Φ 5 mil 250 µm pitch 10 mil	125 µm Φ 250 µm pitch
Thermal Vias, 215 µm Tape	250 µm Φ 10 mil 500 µm pitch 20 mil	180 µm Φ 300 µm pitch	180 µm Φ 300 µm pitch
Distance, Conductor to Edge	250 µm min. 10 mil	175 µm min.	125 µm min.
Ground/Power Plane Coverage	Grid: 40% Metal Localized: 100%	Grid: 60% Metal Localized: 100%	Grid: 60% Metal Localized: 100%
Minimum Tape Layer Count or Minimum Thickness	8 Layers or 1 mm, Whichever is More	8 Layers or 1 mm, Whichever is More	8 Layers or 1 mm, Whichever is More

Notes: a) Typical with current tooling. Custom tooling will allow a maximum fired size of 160 x 160 mm.
More complex size and shape designs can be addressed on an individual basis.
b) Up to 60 layers are possible with alternative processing techniques.
c) All photolithographic processes expected online spring 2003.

Electroplating, electroless plating, and etching

> As a vertically integrated facility, Amitron offers electroplating (Ni/Au and Ni/Pb-Sn), electroless plating (Ni/Au), and etching post-process capabilities to enhance product robustness as well as to overcome specific design or process issues.

> Plated designs must employ a mixed metal material system. Etched designs may be gold, silver, or mixed metal material systems.

> Preferred etched designs employ 50 µm lines and spaces. Minimum lines and spaces are 20 µm.

> Maximum metal thickness using electroplating is 50 µm. Maximum metal thickness using electroless plating is 20 µm.

Passive elements

> Inductors, resistors, and capacitors may all be integrated into a standard LTCC structure. Electrical characteristics are achieved through a combination of design (e.g., surface real estate, one or more layers), inherent properties of the green tape, and the material system chosen.

> Depending upon the material system, enhancement materials exist to locally increase the dielectric constant for some capacitor ranges. Specifics must be reviewed on a design-by-design basis.

> Buried resistors will exhibit a tolerance of +30%. Surface resistors may typically be laser trimmed using a Nd:YAG laser to +2% to +5%. Tighter tolerance requirements must be reviewed on a design-by-design basis. Resistor values are limited by design and material availability, but typically run between 10 Ω and 100 kΩ for buried resistors, and 1 Ω to 100 MΩ for surface resistors. Minimum buried resistor size is 750 x 750 µm; minimum surface resistor size is 500 x 500 µm.

> Overcoat and solder-blocking materials are available only as post-fired operations.

Testing

> DC electrical testing can be achieved with either an electrical Net test (opens and shorts) or a capacitor TAC test. It is preferred that the customer supply an ASCII Netlist indicating Nets (by name or number) along with XY coordinates. A print or file must indicate the part (0,0) location for the Netlist as well as the units for the XY coordinates (inches, mils, metric). If a Netlist cannot be supplied by the customer, Amitron can extract a Netlist from supplied CAD files.

> Amitron employs a Nd:YAG laser trim system for resistive and capacitor element trimming. This equipment is also capable of active trimming or non-standard testing with the appropriate equipment. Please contact the appropriate engineering personnel when such trimming and testing are required.

Singulation

> Primary methods for component singulation are: laser machining, diamond saw, and hot-knife green cutter. Singulation may use one or any combination of these options to produce the final product. All of these singulation options are available at Amitron.

> Except by design, CO_2 laser machining requires a minimum of 1500 µm of non-active area surrounding the active final circuit. A minimum of two optical alignment features parallel to a cut edge must exist on each circuit. These features may be two ends of a single trace, independent targets within the circuit, or optical features in the non-active area close to the active area. CO_2 laser machining offers the highest accuracy of outside product dimensions to internal pattern locations. Accuracy from part edge to the top metal pattern of +50 µm is typical.

> Except by design, a high-speed diamond saw requires a minimum of 1000 µm of non-active area surrounding the active final circuit. A minimum of two optical features in each axis parallel to the final product cut edges are required. These targets must be in the inactive area of the panel near the borders. Accuracy of the final part size is typically 50 µm, but the accuracy of the top metal pattern to the part edge is typically +150 µm. Castellation creation is generally achieved through cavity operations with a dicing saw final segmentation.

> Except by design, a hot-knife green cutter requires 750 µm of non-active area surrounding the active final circuit. A minimum of two optical features in each axis parallel to the final product cut edges is required. These targets must be in the inactive area of the panel near the borders. Accuracy of the final part size and the top metal pattern to the part edge is typically +125 µm.

Cavities

> Cavities are defined as openings or through-holes in the LTCC structure that are introduced into the green state structure prior to firing. Post-machined operations (CO_2 laser drilling, ultrasonic milling, etc.) are not included in the recommendations below.

> Minimum distance between adjacent cavities or through-holes, or between cavity walls or though-holes and the part edge, is 2500 µm.

> Minimum cavity length and width are 2500 µm. Maximum ratio of cavity depth to minimum XY dimension is 1:1. Preferred ratio is 1:2. Minimum radius on any corner of a cavity is 500 µm.

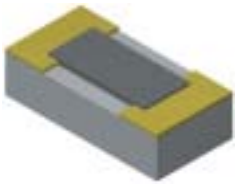
> Cavities with floors must have a minimum floor thickness of 1000 µm. Via and conductor limitations related to cavity walls or cavity shelves are the same as those listed on page 13, “Vias,” paragraph 3, and page 14, “Conductors,” paragraphs 1 through 3.

> Cavities may have one or more intermediate shelves. Minimum shelf thickness is 1000 µm. Minimum shelf width is 1200 µm.

> Maximum combined surface area of cavity opening to total part surface area is 60%. Preferred maximum ratio is 40%.

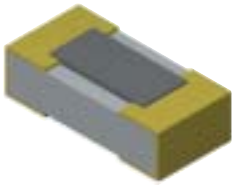
Style 1: Top contact, no wrap

Pads on resistor side only; use with wire-bonding; back-side metallization optional



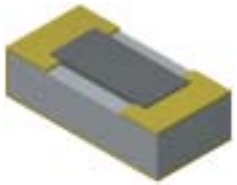
Style 2: Dual wrap

Common surface mount style; both terminations wrap around from resistor side to backside; solder or epoxy attach



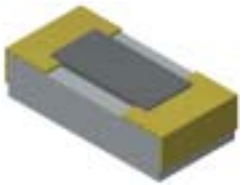
Style 3: Single wrap

One termination wraps from resistor side to full coverage on backside; attach wire to the other termination; use as a terminator or to increase thermal contact



Style 4: Partial wrap

Both terminations wrap around from resistor side partially down the edge of the chip; use as a flip chip; edge metal gives good mechanical bond (fillet); reduced capacitance



Listed on the following page are some of the more common chip sizes, styles, and terminations that Amitron provides. If you do not find what you're looking for, call with your particular needs!

> **Sizes as small as 20 x 20 mils** (0.5 x 0.5 mm)

> **Wide resistance range,** from approximately 0.2 Ω to 50 GΩ. There are some limitations on size, tolerance, and TCR at the ends of these ranges.

> **Tolerance to 1%,** with tolerances to 0.1% available in some instances

> **Amitron is QPL listed** per MIL-PRF-55342. See the QPL or call for specifics.

> **Termination materials** include:

- Gold for wirebonding
- Platinum-gold, palladium-silver for soldering or conductive epoxy attachment
- Tin-lead plate, gold plate for soldering. These terminations consist of three layers: a plateable silver, a solderable nickel barrier layer, and the outer plated layer.
- Optional solder tinning. In addition to the plating options, a relatively thick printing of solder (tin-lead or gold-tin) can be added on the mounting surface only.

> **Hi-rel processing is also available,** adding 100% thermal shock

THE INDUSTRY'S SMALLEST WIRE-BONDABLE CHIP RESISTOR is available in two styles, 20 x 20 mils

STYLE 1: 20 X 20 mils, top contact
two top wirebond contacts, optional backside metal

STYLE 3: 20 X 20 mils, back contact
only one wirebond required, backside metal is second contact

Chip resistor sizes & specifications (use metric size for ordering)

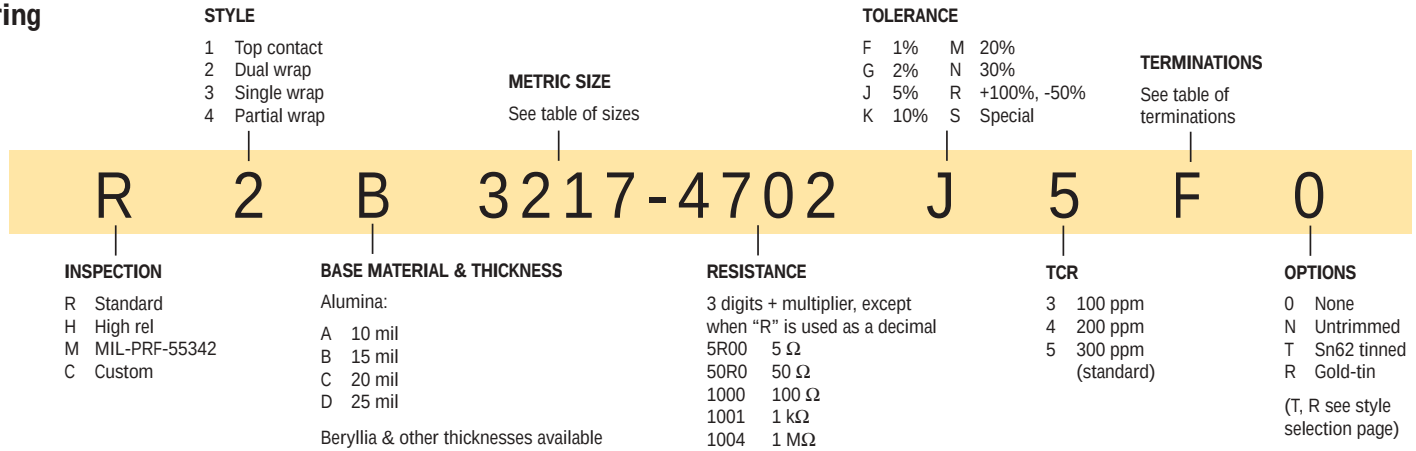
Inch size code	Length (inch)	Width (inch)	Metric size code	Length (mm)	Width (mm)	Power (W) T_A=70ºC	Voltage (V)
0202	0.020	0.020	**0505**	0.51	0.51	0.250	30
0302	0.030	0.020	**0805**	0.76	0.51	0.060	24
0402	0.040	0.020	**1005**	1.02	0.51	0.080	32
0502	0.050	0.025	**1306**	1.27	0.64	0.125	40
0504	0.050	0.040	**1310**	1.27	1.02	0.200	40
0505	0.050	0.050	**1313**	1.27	1.27	0.250	40
0603	0.060	0.030	**1508**	1.52	0.76	0.180	48
0705	0.075	0.050	**1913**	1.91	1.27	0.280	60
0805	0.080	0.050	**2013**	2.03	1.27	0.280	60
1005	0.100	0.050	**2513**	2.54	1.27	0.375	80
1010	0.100	0.100	**2525**	2.54	2.54	0.750	80
1206	0.125	0.065	**3217**	3.18	1.65	0.600	100
1505	0.150	0.050	**3813**	3.81	1.27	0.560	120
2010	0.200	0.100	**5125**	5.08	2.54	1.500	160
2512	0.250	0.125	**6432**	6.35	3.18	2.300	200

Available termination materials and codes

Resistor Surface	Back Surface	Style 1	Style 2	Style 3	Style 4
Au	none	A			A
Pt-Au	none	B			B
Pd-Ag	none	C			C
Sn-Pb plate	none	D			D
Au plate	none	P			P
Au	Au	G	G	G	
Pt-Au	Pt-Au	H	H	H	
Pd-Ag	Pd-Ag	L	L	L	
Sn-Pb plate	Sn-Pb plate	J	J	J	
Au plate	Au plate	K	K	K	
Au	Pt-Au	E		E	
Au	Pd-Ag	F		F	

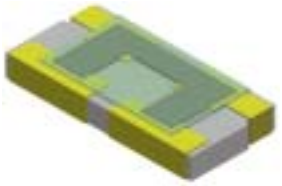
A metallized back surface on Style 1 chips is not connected to either resistor termination. On Style 3 chips, the back surface metallization material is the same as the wrapped resistor termination.

Part numbering



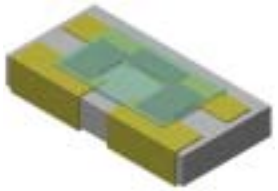
Style A: Dual wrap I/O pads

Shunt attenuator (pi-pad) with wrap-around I/O's and grounds for solder attach



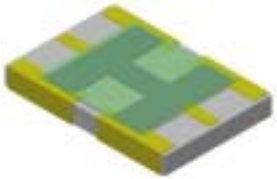
Style P: Top contact I/O with ground wrap

Shunt attenuator with wirebond I/O pads and wrap-around grounds for conductive epoxy attach



Custom styles...

... such as this dual-shunt attenuator with wirebond I/O's and wrap-around grounds; parts can be designed to meet your requirements



Amitron attenuators are summarized as follows. If you do not see what you require, please do not hesitate to contact us to explore alternative solutions that may suit your particular needs!

> Characterized to 18 GHz

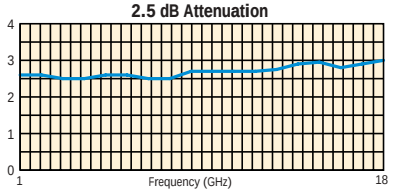
> Rated 0.125 W, 25 V at T_A = 70°C

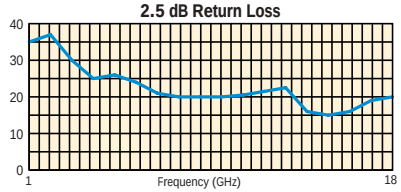
> Termination materials include:

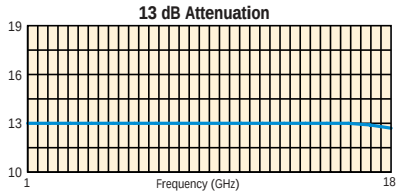
- Gold for wirebonding
- Platinum-gold, palladium-silver for soldering or conductive epoxy attachment
- Tin-lead plate, gold plate for soldering. These terminations consist of three layers: a plateable silver, a solderable nickel barrier layer, and the outer plated layer.
- Optional solder tinning. In addition to the plating options, a relatively thick printing of solder (tin-lead or gold-tin) can be added on the mounting surface only.

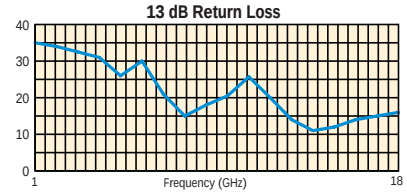
> Hi-rel processing is also available, adding 100% thermal shock.

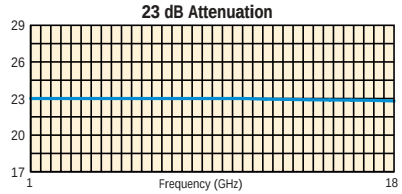
TYPICAL PERFORMANCE DATA

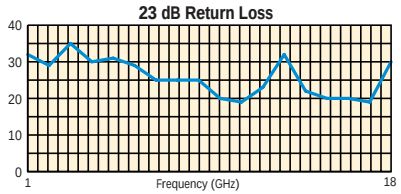






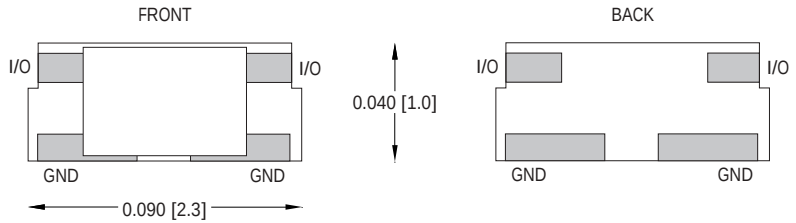




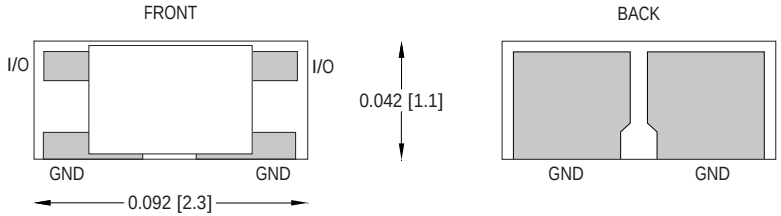


Chip attenuator sizes (use metric size for ordering)

STYLE A
size code 2310



STYLE P
size code 2311



Available termination materials and codes

I/O	Backside Ground	Style A	Style P
Au	Au	G	G
Pt-Au	Pt-Au	H	H
Pd-Ag	Pd-Ag	L	
Sn-Pb plate	Sn-Pb plate	J	
Au plate	Au plate	K	
Au	Pt-Au		E
Au	Pd-Ag		F

Part numbering

STYLE
A Dual wrap
P Ground wrap

METRIC SIZE
See above

TOLERANCE
F 1%

TERMINATIONS
See table of terminations

R P A 2311-6R00 F 5 H 0

INSPECTION
R Standard
H High rel
C Custom

BASE MATERIAL & THICKNESS
Alumina:
A 10 mil (standard)
B 15 mil
C 20 mil
D 25 mil

Beryllia & other thicknesses available

ATTENUATION
3 digits + "R" is used as a decimal
R500 0.5 dB
5R00 5 dB
16R0 16 dB

TCR
3 100 ppm
4 200 ppm
5 300 ppm (standard)

OPTIONS
0 None
T Sn62 tinned
R Gold-tin

(T, R see style selection page)

Amitron highlights!

- > Multilayer, double-sided thick film substrates
- > Diffusion patterning for reduced via size and spacing in multilayers
- > Lower-cost microwave circuitry, featuring advanced etching technology
- > LTCC substrates up to 30 layers
- > Etched line width and spacing — controlled to an order of magnitude better than traditional screen printing for lower-loss, higher-density circuits
- > Alumina substrates 96%, 99.5%, and 99.6%
- > Ferrite, beryllia, aluminum-nitride substrates
- > Lines and spaces to 1 mil
- > Edge wraps and metallized substrate vias
- > In-house plating: gold, tin-lead, nickel
- > Specific metallizations for wire bonding, soldering, or brazing
- > Integrated laser-trimmed resistors
- > Integrated capacitors, inductors, and thermistors
- > Machining of substrates to any shape
- > Proprietary method for creating structures with blind features such as open cavities and counterbores
- > Net testing
- > ISO 9002 registered facility
- > Vertical integration: All processes from CAD to shipped product are performed in-house
- > Microwave design assistance from Anaren headquarters as needed
- > Circuit layout assistance
- > Extensive industry experience in materials, ceramics, and microelectronics design
- > Standard and custom chip resistors and attenuators, plus QPL-listed chips per DESC MIL-PRF-55342

We're ready to help!

Whatever you're thinking, we're ready with information, design assistance, samples, quotations — anything and everything you need to develop those never-before-possible solutions. Simply call us at 978-686-1882, e-mail us at ceramics@anaren.com, or visit www.anaren.com.

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What'll we think of next?™